CLAIMS:

What is claimed is:

1. A method for modifying computer program instructions during execution of those instructions, the method comprising computer-implemented steps of:

writing a first value into a memory location, wherein the first value represents a first instruction, and wherein the first instruction is a patch class instruction;

fetching the first instruction from the memory location;

executing the first instruction; and

overwriting a second value into the memory location, wherein the second value represents a second instruction, and wherein the second instruction is a patch class instruction;

wherein the overwriting may be concurrent with the execution of the first instruction.

2. The method according to claim 1, further comprising:

refetching the first instruction from the memory location; and

reexecuting the first instruction

3. The method according to claim 1, further comprising:

fetching the second instruction from the memory location; and

executing the second instruction.

4. The method according to claim 1, further comprising:

reconciling a processor's execution pipeline with

the memory location, wherein the reconciliation ensures that the second instruction will be fetched and executed from the memory location if the program subsequently returns to that memory location.

5. The method according to claim 1, wherein the patch class instructions include no-operation instructions and branch instructions.

6. The method according to claim 1, wherein the steps are implemented in a multiprocessor computer system.

7. The method according to claim 1, wherein the steps are implemented in a uniprocessor computer system.

8. A computer program product in a computer readable medium for use in a data processing system, for modifying computer program instructions during execution of those instructions, the computer program product comprising:

instructions for writing a first value into a memory location, wherein the first value represents a first instruction, and wherein the first instruction is a patch class instruction; and

instructions for overwriting a second value into the memory location, wherein the second value represents a second instruction, and wherein the second instruction is a patch class instruction;

wherein the overwriting may be concurrent with the execution of the first instruction.

9. The computer program product according to claim 8, further comprising:

instructions for reconciling a processor's execution pipeline with the memory location, wherein the reconciliation ensures that the second instruction will be fetched and executed from the memory location if the program subsequently returns to that memory location.

10. The computer program product according to claim 8, wherein the patch class instructions include no-operation instructions and branch instructions.

11. The computer program product according to claim 8, wherein the steps are implemented by a multithreaded program.

12. The computer program product according to claim 8, wherein the steps are implemented by a single-threaded program.

13. A system for modifying computer program instructions during execution of those instructions, the system comprising:

a writing component which writes a first value into a memory location, wherein the first value represents a first instruction, and wherein the first instruction is a patch class instruction;

a fetching component which fetches the first instruction from the memory location;

a processing component which executes the first instruction; and

an overwriting component which overwrites a second value into the memory location, wherein the second value

represents a second instruction, and wherein the second instruction is a patch class instruction;

wherein the overwriting may be concurrent with the execution of the first instruction.

14. The system according to claim 13, further comprising:

a refetching component which refetches the first instruction from the memory location; and

a processing component which reexecutes the first instruction.

15. The system according to claim 13, further comprising:

a fetching component which fetches the second instruction from the memory location; and

a processing component which executes the second instruction.

16. The system according to claim 13, further comprising:

a reconciliation component which reconciles a processor's execution pipeline with the memory location, wherein the reconciliation ensures that the second instruction will be fetched and executed from the memory location if the program subsequently returns to that memory location.

17. The system according to claim 13, wherein the patch class instructions include no-operation instructions and branch instructions.

18. The system according to claim 13, wherein the components are part of a multiprocessor computer system.

19. The system according to claim 13, wherein the components are part of a uniprocessor computer system.